# PIPELINE ANALOG-TO-DIGITAL CONVERTER

## Field of the Invention

The present invention is related to the field of analog-to-digital

5    converters. In particular, the present invention is related to a method and apparatus

directed to a multi-stage pipeline analog-to-digital converter with reduced differential

non-linearity (DNL) and/or integral non-linearity (INL) based conversion errors.


## Background of the Invention

An analog-to-digital converter (ADC) is a device that takes an analog

10    data signal and converts it into a digital code, i.e. digitizes or quantizes the analog

signal. An ADC is a key building block in mixed-mode integrated circuits (ICs). Once

the analog signal is converted into the digital domain, complicated signal processing

functions can be performed with easier handling and improved noise immunity. In some

instances, power dissipation can be reduced since many ADCs are implemented in a

15    deep submicron CMOS process.

ADCs may employ a wide variety of architectures, such as the

integrating, successive-approximation, flash, and the delta-sigma architectures.

Recently, the pipelined analog-to-digital converter (ADC) has become a popular ADC

architecture for use in high-speed applications such as CCD imaging, ultrasonic medical

20    imaging, digital video, and communication technologies such as cable modems and fast

Ethernet. Pipelined ADCs are typically chosen because of their high accuracy, high

throughput rates, and low power consumption. Moreover, the pipeline architecture

generally provides better performance for a given power and semiconductor die area

than other ADC architectures.

25    An example of a conventional k-stage pipelined ADC (100) is shown in

FIG. 1. As shown in the figure, the conventional k-stage pipelined ADC (100) includes

an array of k gain stages (102) and a decoder logic circuit (104). Each of the gain stages

(102) is connected in series to the previous gain stage (102). Each gain stage (102) is

also connected to the decoder logic circuit (104).

In operation, an analog input voltage (Vin) is provided to the first gain stage (102). The first gain stage (102) samples the analog input voltage (Vin) and converts it to a first digital coefficient (n1). The first coefficient (n1) is processed by the decoder logic circuit (104) to provide the Most Significant Bit (MSB) of a digital data representation of the analog input voltage (Vin). The first gain stage (102) also converts the first digital coefficient (n1) back to an analog representation. The analog representation is subtracted from the sampled analog input voltage (Vin) and multiplied by a gain multiplier to provide a residue voltage. The residue voltage (Vres (1)) from the first gain stage (102) becomes the analog input voltage to the next gain stage (102) of the pipeline. That is, Vin (2) = Vres(1). The residue voltage (Vres(i)) continues through the pipeline of gain stages (102), providing another digital coefficient (ni) based on the digital representation of the input to that gain stage, as described above.

The overall digital representation of the analog voltage input (Vin) is obtained by concatenating the k digital coefficients (n1 through nk) from the array of k gain stages (102) through the decoder logic circuit (104). Digital error correction logic is typically used to improve the accuracy of conversion by providing overlap between the quantization ranges of adjacent gain stages (102) in the pipeline. An architecture that makes use of this correction to a 1-bit per stage pipeline ADC is a 1.5-bit per stage pipeline topology.

FIG. 2 is a graph illustrating ideal transfer characteristics of a 1.5-bit per stage conventional pipeline ADC such as illustrated in FIG. 1. In the 1.5-bit architecture, there are two thresholds or transition points in the transfer curve, resulting in three operating regions. Each stage of the 1.5-bit architecture effectively converts only one bit of information. The extra region (as compared to a 1-bit per stage topology) is used for redundancy. That is, the extra bit of information is combined with the digital outputs from subsequent gain stages (102) in the pipeline to generate another bit.

As shown in FIG. 2, the input voltage (Vin) appears along the x-axis and illustrates that the resolvable input range of the ADC is given by: -Vref < Vin < +Vref. Two transition points appear along the x-axis. The first transition point occurs at Vin equal to -Vref/4 and the second transition point occurs at Vin equal to +Vref/4. The two

transition points divide the operating range for the input voltage (Vin) into three operating regions, where two bits (00, 01, and 10) of the digital output of each stage characterize the entire range. Further, the slope of each curve reflects the gain multiplier employed in the gain stage (102) of FIG. 1.

5         Operationally, the gain stage (102) examines the input (Vin (i)) and determines whether the input is less than the first transition point, -Vref/4. If Vin(i) is less than the first transition point (-Vref/4) then the digital code output for the gain stage (102) is 00. Similarly, a digital output code of 01 is generated for Vin(i) between the first transition point, -Vref/4, and the second transition point (+Vref/4). If Vin(i) is

10   greater than the second transition point, +Vref/4, the ideal transfer characteristics generates a digital output code of 10.

Moreover, the output residue voltage (Vres(i)) is generated by the following transfer function:

$$Vres(i) = 2M \cdot Vin(i) - Di \cdot Vref \qquad\qquad (EQ\ 1)$$

15   where M is the number of effective bits that are being generated by stage i, 2M represents the gain multiplier for the gain stage (102), and Di is a constant determined by the digital representation of the analog input voltage (Vin), having possible values of -1, 0, and 1. For the 1.5-bit per stage ADC, the number of effective bits (M) is one. The output residue voltage (Vres(i)) generated at the ith gain stage (102) becomes the analog

20   input voltage (Vin (i+1)) to the next gain stage (102).


## Brief Description of the Drawings

Non-limiting and non-exhaustive embodiments of the present invention are described with reference to the following drawings.

FIG. 1 illustrates a schematic block diagram of a conventional pipelined

25   analog-to-digital converter (ADC); and

FIG. 2 illustrates a graph of an ideal transfer curve for the conventional pipelined analog-to-digital converter (ADC) of FIG. 1.

FIG. 3 illustrates an example schematic diagram of an ADC converter system that is arranged in accordance with the present invention.

FIG. 4 illustrates a schematic diagram for a first stage converter circuit that is arranged in accordance with the present invention.

FIG. 5 illustrates the timing of various operational phases for the first stage converter circuit illustrated in FIG. 4.

5         FIG. 6 illustrates a simplified diagram of an example MDAC circuit that is arranged in accordance with the present invention, while operated during a sampling phase.

FIG. 7 illustrates a simplified diagram of an example MDAC circuit that is arranged in accordance with the present invention, while operated during an

10       amplification phase.

FIGS. 8 - 10 illustrate various performance merits of a pipelined converter circuit that is arranged in accordance with the present invention.

## Detailed Description of the Preferred Embodiment

Various embodiments of the present invention will be described in detail

15       with reference to the drawings, where like reference numerals represent like parts and assemblies throughout the several views. Reference to various embodiments does not limit the scope of the invention, which is limited only by the scope of the claims attached hereto. Additionally, any examples set forth in this specification are not intended to be limiting and merely set forth some of the many possible embodiments for

20       the claimed invention.

Throughout the specification and claims, the following terms take at least the meanings explicitly associated herein, unless the context clearly dictates otherwise. The meanings identified below are not intended to limit the terms, but merely provide illustrative examples for the terms. The meaning of "a," "an," and "the"

25       includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means either a direct electrical connection between the items connected or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a single

30       component or a multiplicity of components, either active and/or passive, that are

coupled together to provide a desired function. The term "signal" means at least one current, voltage, charge, temperature, data, or other signal.

Briefly stated, the invention is related to an apparatus and method for a pipelined ADC to minimize DNL and INL error using reference pre-sampling. An example first stage in the pipelined converter includes a sample/hold amplifier (SHA) circuit, an evaluator circuit, and a multiplying digital-to-analog converter (MDAC) circuit. The evaluator circuit evaluates the input signal in the converter while the SHA circuit samples the input signal. The MDAC samples the SHA output at substantially the same time it samples a reference voltage, where the reference voltage is adjusted in response to the output of the evaluator circuit. Errors due to capacitor mismatching are minimized such that the settling characteristics of the various amplifiers in the circuits dominate the DNL/INL performance.

Pipelined ADCs may be implemented with switched capacitor circuit techniques, allowing for easy storage and amplification of analog signals in a CMOS based process. DNL and INL measurements are obtained to determine the linearity characteristics of the ADC by measuring the differences between the actual step widths and a step width for an ideal least significant bit (LSB) of the converter. INL error is defined by the difference between the actual transfer curve of the converter and the ideal transfer curve, and is measured with integrating DNL. An ideal ADC has an analog step size equal to 1-LSB resulting in a DNL and INL of 0-LSB. The resolution of 1-LSB is determined by the full scale voltage range of the converter (VFS) as $VFS/2^N$, where N corresponds to the resolution of the ADC.

The DNL and INL characteristics of an ADC are related to the settling time of the conversion process. For example, the amplifier in the ADC has a finite bandwidth and a finite output drive characteristic (e.g., a maximum current output drive) that directly impacts the settling time in the conversion process. For this example, the amplifier may provide inaccurate conversion results when the output signals of the amplifier have not completely settled. The settling time problem could be resolved with a high DC gain and/or a wide bandwidth amplifier. However, DNL and INL characteristics can be directly related to the capacitor matching due to process

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related variations. The present invention overcomes the process imperfections with early input signal monitoring and reference pre-sampling such that DNL and INL error is predominately dependent on the amplifier settling performance and not on capacitor matching.

5        FIG. 3 illustrates an example schematic diagram of an ADC converter system (300) that is arranged in accordance with the present invention. The ADC converter system (300) includes a first stage converter circuit, subsequent stage converter circuits (second stage through last stage), and a decoder logic circuit. The first stage converter circuit is arranged to receive an analog input signal (VIN) and

10    provide an analog output signal (VOUT1) to the subsequent stage converters. Each of the converter stages (first, second ... last) are arranged to cooperate with the decoder logic circuit. The decoder logic circuit is arranged to determine the digital output code (DOUT) from the various control signals (CTL1, CTL2 ... CTLK) for each conversions stage, and from the residue of the last stage of the converter (VRESK).

15        An example first stage converter includes a sample and hold amplifier (SHA) circuit, a multiplying digital-to-analog converter (MDAC) circuit, and an evaluator circuit. The SHA circuit may be implemented as either separate sampler and gain circuits, or as a circuit where sampling and gain functions are integrated into a single functional block (e.g., switched capacitor SHA). The gain circuit may provide a

20    signal gain that is less than unity, unity, or greater than unity as may be desired in a particular implementation.

       A switched capacitor circuit can be arranged to provide the MDAC functions by amplifying an input signal with a DC level (reference voltage) shift. The actual input signal is amplified by the signal transfer factor of the MDAC, which

25    includes capacitors, switching circuits, and an amplifier. The MDAC output is provided within the range of the voltage reference by means of a DC level subtraction or addition. The output conversion of the MDAC is decided by a sub-ADC such as a flash-type converter. Flash-type low resolution ADCs can be used in the pipeline ADC since the sub-ADC offset can be corrected by digital correction logic with an adder

30    array.

The linearity of the MDAC conversion is dependent on: capacitor matching, DC gain of the amplifier in the MDAC, and bandwidth of amplifier in MDAC. DNL characteristics of the MDAC can be improved by utilizing a multi-bit MDAC (e.g., 1.5-bit, 2-bit, 2.5-bit, etc.). The sampling capacitor size of a single-bit MDAC is the same as that for a multi-bit MDAC. The sampling capacitor size is limited by thermal noise levels and/or process dependent capacitor matching characteristics. The total sampling capacitor size ($C_{TOTAL}$) in the MDAC can be determined, to a first order, by the thermal noise level as follows below. C corresponds to a unit capacitor size and $\Delta C_i$ corresponds to the mismatch in the $i^{th}$ sampling capacitor.

$$OUTPUT_{MDAC} = \frac{C_{TOTAL}}{C + \Delta C_i} \cdot INPUT \qquad (Eq.1)$$

$$OUTPUT_{MDAC} = \frac{C_{TOTAL}}{C + \Delta C_i} \cdot \frac{C}{C_{TOTAL}} = \frac{1}{(1 + \frac{\Delta C_i}{C_i})} \approx 1 - \frac{\Delta C_i}{C_i} \qquad (Eq.2)$$

The input equivalent error ($ERROR_{INPUT}$) is related to the bit resolution (m) of the MDAC, the unit capacitor size (C), and the mismatching of the $i^{th}$ sampling capacitor ($\Delta C_i$):

$$ERROR_{INPUT} = \frac{\Delta C_i}{C} \cdot \frac{1}{2^m} \qquad (Eq.3)$$

The DNL error of the $1^{st}$ stage MDAC is determined by the input equivalent error ($ERROR_{INPUT}$) and the amplification factor of the MDAC ($2^N$, where N corresponds to the number of bits of resolution in the ADC system) as:

$$DNL = \frac{\Delta C_i}{C} \cdot \frac{1}{2^m} \cdot 2^N \qquad (Eq.4)$$

The total size of the sampling capacitor ($C_{TOTAL}$) can be fixed for lower power dissipation based on the thermal noise level as:

$$C = \frac{C_{TOTAL}}{2^m} \qquad (Eq.5)$$

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Matching error in the capacitors ($\Delta C_i$) is dependent on the unit sampling capacitor size (C) and a process related matching coefficient (k) as:

$$\Delta C_i = k \cdot \sqrt{C} \qquad\qquad\qquad\qquad\text{(Eq.6)}$$

The DNL error is determined by substituting Eq.5 and Eq.6 into Eq.4, such that:

$$DNL = k \cdot \frac{1}{\sqrt{C_{TOTAL}}} \cdot 2^{N - \frac{m}{2}} \qquad\qquad\text{(Eq. 7)}$$

The DNL error is improved by a factor of $\sqrt{2}$ with every extra bit of resolution in each stage of the pipelined converter.

Although multiple bits are preferred for each stage of the pipelined converter to reduce DNL error, higher operating frequencies require higher speed amplifiers in each stage. The higher operating frequency of the amplifier results in higher power dissipation which may be unacceptable in certain applications. As such, 1.5 bits per stage may be preferable in the ADC to limit power dissipation, reduce amplifier requirements and to minimize DNL error.

DNL error can be further reduced by using a capacitor swapping technique in the 1.5 bit stage. Two sampling capacitors (e.g., C1 and C2) and an amplifier can be arranged to operate as part of a 1.5 bit-per-stage MDAC. During the sampling phase, the top plates of both capacitors are coupled to the positive input node of the amplifier, while the bottom plates of both capacitors are coupled to the input signal. The top plates are also coupled to a ground signal in the sampling phase such that the input signal is stored on the capacitors. During the amplification phase, the bottom plate of one capacitor (e.g., C1) is connected to the amplifier output, while the bottom plate of the other capacitor (e.g., C2) is connected to a reference voltage level. A 1.5-bit sub ADC (e.g., two comparators) evaluates the sampled input signal to perform 1.5 bit analog-to-digital conversion. The comparison points for the 1.5-bit sub ADC is, for example, -1/4 and +1/4 of a reference voltage level for the 1.5-bit sub ADC. The reference voltage levels for the MDAC correspond to, for example, -1V, 0V, and +1V based on the 1.5-bit sub ADC conversion, and are utilized to maximize the correction range for comparator offsets via the digital correction logic.

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During the amplification phase, one of the capacitors (e.g., C1) is used as sampling capacitor while the other capacitor (e.g., C2) is used as feedback capacitor. The selection of the sampling capacitor and the feedback capacitor is determined by the input signal level as evaluated during the sampling phase. In one example, the input

5    signal level is evaluated as less than ¼ of the reference voltage level and capacitor C1 is used as the feedback capacitor while capacitor C2 is used as the sampling capacitor. In another example, the input signal is evaluated as between the range of + ¼ and − ¼ of the reference voltage level and capacitor C2 is used as the feedback capacitor while capacitor C1 is used as the sampling capacitor. In still another example, the input signal

10   level is evaluated as greater than ¼ of the reference voltage level and capacitor C1 is used as the feedback capacitor while capacitor C2 is used as the sampling capacitor. The output voltage ($V_{OUT}$) for the MDAC is determined by the input signal level ($V_{IN}$) as follows:

For VIN < -¼ ·VREF,

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$$V_{OUT} = \left(1 + \frac{C_2}{C_1}\right) \cdot V_{IN} + \frac{C_2}{C_1} \qquad \text{(Eq.8)}$$


For -¼ ·VREF < VIN < +¼ ·VREF,

$$V_{OUT} = \left(1 + \frac{C_1}{C_2}\right) \cdot V_{IN} \qquad \text{(Eq.9)}$$


20                    For VIN > +¼ ·VREF,

$$V_{OUT} = \left(1 + \frac{C_2}{C_1}\right) \cdot V_{IN} - \frac{C_2}{C_1} \qquad \text{(Eq.10)}$$

The DNL error of 1.5bit MDAC without the capacitor swapping caused by the capacitor mismatch is 2·α, where the sampling capacitor ($C_S$) is given as $C_S = C_1$, = C· (1 + α), the feedback capacitor ($C_F$) is given by $C_F = C_2 = C \cdot (1 - α)$, and α

25   corresponds to the capacitor mismatching coefficient. However, the DNL error with the capacitor swapping is improved by 2 times and α. Although the multi-bit stage ADC theoretically has better DNL and INL performance, the 1.5-bit per-stage ADC may be

preferable since it has the advantages of: high speed operation, lower power dissipation, and can have improved DNL performance with the addition of the above described capacitor swapping technique.

Although DNL performance can be improved using the capacitor
5    swapping techniques, the DNL performance is highly dependent on capacitor matching. Capacitor mismatches may result in the ADC performance having missing codes and/or be non-monotonic. Additionally, INL performance does not necessarily improve in ADCs that utilize the capacitor swapping technique. The lack of improvement in the INL performance is predominantly a result of the signal transfer curves being different
10   at the tripping points because the capacitor swapping technique changes the ADC transfer curves based on the input signal level to reduce DNL error.

In the previously described 1.5-bit MDAC, the imperfect capacitor matching causes transfer curve errors as well as dropping voltage error around the transfer curve trip points. However, the non-ideal transfer curve of the MDAC in the
15   first stage does not contribute to DNL related errors since the DNL errors relate to the dropping voltage errors around the transfer curve trip points. Thus, there is relatively insignificant INL errors due to capacitor mismatches even if the dropping voltages around the trip points are the same as the ideal dropping voltage

The dropping voltage is related to the sampling capacitor ($C_S$), the
20   feedback capacitor ($C_F$), and the reference voltage level ($V_{REF}$) as ($C_S/C_F$) · $V_{REF}$. By sampling the reference voltage level ($V_{REF}$) with the feedback capacitor ($C_F$), the dependency for the dropping voltage on capacitor matching can be reduced.

FIG. 4 illustrates a schematic diagram for a first stage converter (400) circuit that is arranged in accordance with the present invention. FIG. 4 includes the
25   functional blocks of the first stage converter that was described with respect to FIG. 3. The example first stage converter circuit (400) includes a sample-and-hold amplifier (SHA) circuit, a multiplying digital-to-analog converter (MDAC) circuit, and an evaluator circuit. An example of the timing related to various signals and functions are illustrated in FIG. 5.

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The SHA circuit includes an amplifier circuit (AMP$_1$), two capacitor circuits (C$_{S1}$, C$_{F1}$), and five switching circuits (S$_1$ – S$_5$). Switching circuits S$_1$, S$_3$, and S$_4$ are responsive to signal Q$_1$, while switching circuit S$_2$ and S$_5$ are responsive to signal Q$_2$. The SHA circuit is responsive to signals Q$_1$ and Q$_2$, which define the operating phases for the sample and hold/amplification modes of the SHA circuit. While signal Q$_1$ is asserted: Capacitor C$_{F1}$ is reset to an initial condition (e.g., 0V) and capacitor C$_{S1}$ is arranged to sample the input signal (V$_{IN}$) via switching circuits S$_1$, S$_3$, and S$_4$. Capacitor C$_{S1}$ is arranged to cooperate with capacitor C$_{F1}$ and switching circuits S$_2$ and S$_5$ such that amplifier AMP$_1$ redistributes the stored charge from capacitor C$_{S1}$ when signal Q$_2$ is asserted.

The MDAC circuit includes an amplifier circuit (AMP$_2$), two capacitor circuits (C$_{S2}$, C$_{F2}$), and five switching circuits (S$_6$ – S$_{10}$). Switching circuits S$_7$ and S$_{10}$ are responsive to signal Q$_1$, while switching circuit S$_6$, S$_8$, and S$_9$ are responsive to signal Q$_2$. The MDAC circuit is responsive to signals Q$_1$ and Q$_2$, which define the operating phases for the MDAC circuit. While signal Q$_2$ is asserted: Capacitor C$_{F2}$ is reset to known condition (e.g., a selected reference voltage level) via switching circuits S$_8$ and S$_9$, and capacitor C$_{S2}$ is arranged to receive the sampled signal (e.g., V$_{SHA}$) via switching circuit S$_6$. Capacitor C$_{S2}$ is arranged to cooperate with capacitor C$_{F2}$ and switching circuits S$_7$ and S$_{10}$ such that amplifier AMP$_2$ redistributes the stored charges from capacitors C$_{F2}$ and C$_{S2}$ when signal Q$_1$ is asserted. The resulting signal output of the MDAC circuit corresponds to VOUT$_1$ as illustrated in FIGURES 8 and 9.

The evaluator circuit includes two comparators (CP$_1$ and CP$_2$), a capacitor (C$_{S3}$), a switching circuit (S$_{11}$), and a logic circuit. Switching circuit S$_{11}$ is responsive to signal Q$_1$, while comparator circuits CP$_1$ and CP$_2$ are responsive to signal Q$_{1B}$, which define the operating phases for the evaluator circuit. Capacitor C$_{S3}$ is arranged to cooperate with switching circuit S$_{11}$ such that the input signal (V$_{IN}$) is sampled by capacitor C$_{S3}$ while signal Q$_1$ is asserted. Signal Q$_{1B}$ is asserted after switching circuit S$_{11}$ decouples capacitor C$_{S3}$ from the input signal (V$_{IN}$). Comparator circuits CP$_1$ and CP$_2$ are arranged to compare the sampled signal from capacitor C$_{S3}$ to reference voltage levels when signal Q1B is asserted. The reference voltage level for

comparator $CP_1$ corresponds to $+ \frac{1}{4}$ of a predetermined reference voltage level, while the reference voltage level for comparator $CP_2$ corresponds to $- \frac{1}{4}$ of the predetermined reference voltage level. The logic circuit is arranged to evaluate the output of the comparators ($CP_1$ and $CP_2$) and provide digital output signals (e.g., $CLT_1$, $OUT_1$). In

5     one example, the digital output signals correspond to multi-bit signals that are utilized by decoder logic (see FIG. 3).

The functions of the comparator circuits ($CP_1$ and $CP_2$) and the logic circuits in the evaluator circuit can be combined into a single functional block. Moreover, a single comparator circuit can be used with a time based multiplexing

10    circuit to accomplish the same functions of comparator circuits $CP_1$ and $CP_2$.

A reference circuit can be arranged to provide the reference level that is utilized by the MDAC. The reference circuit is responsive to at least one of the outputs of the evaluator circuit (e.g., $CTL_1$), which may correspond to one or more control bits. The reference circuit may also be arranged to provide the reference levels that are

15    utilized by the comparator circuits in the evaluator circuit.

The example circuit illustrated in FIG. 4 can be used in a 1.5-bit 1st stage of a pipelined ADC. The circuit is arranged to provide reference pre-sampling in the MDAC circuit as will be described with reference to FIG. 4 and FIG. 5. The SHA circuit provides sample and hold functions with respect to the analog input signal ($V_{IN}$)

20    to improve the dynamic performance of the converter. The evaluator circuit is arranged to operate as a 1.5-bit flash ADC. In one example, the sampling capacitor ($C_{S2}$) in the MDAC circuit is approximately two times bigger than the feedback capacitor ($C_{F2}$) such that the signal transfer gain in the MDAC circuit has a gain of roughly two.

The operation of a conversion cycle for the circuit illustrated in FIG. 4

25    will be described below with reference to the signal waveforms illustrated in FIG. 5. FIG. 6 illustrates a simplified diagram of an example MDAC circuit during a sampling phase, while FIG. 7 illustrates a simplified operational diagram of the example MDAC circuit during an amplification phase.

The input signal ($V_{IN}$) is sampled on the sampling capacitor ($C_{S1}$) in the

30    SHA circuit during the sampling phase which is initiated by signal $Q_1$. The input signal

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($V_{IN}$) is also sampled on the input sampling capacitor ($C_{S3}$) of evaluator circuit. The evaluator circuit compares the input signal level to the reference levels (e.g., VREF/4, -VREF/4) and provides a digital output code (e.g., CTL1, OUT1) at the beginning of the amplification phase which is initiated by signal $Q_2$.

5    The reference voltage for the MDAC circuit is adjusted in response to at least one of the digital output codes from the evaluator circuit. For the example illustrated in FIG. 6, the reference voltages are selected from the set of: +REF, 0V, and –REF in response to the evaluator circuit output. As illustrated in FIG. 6, the reference voltage for the MDAC circuit ($V_{REFMD}$) and the output of the SHA circuit ($V_{SHA}$) are

10 sampled while signal $Q_2$ is asserted (the amplification phase), where the feedback capacitor (e.g., $C_{F2}$ from FIG. 4) samples $V_{REFMD}$ and the sampling capacitor (e.g., $C_{S2}$ from FIG. 4) samples $V_{SHA}$. During the amplification phase, the sampled signals ($V_{SHA}$ and $V_{REFMD}$) are amplified as illustrated in FIG. 7.

    The input signal ($V_{IN}$) is monitored a half clock cycle in advance as

15 compared to conventional methods such that an appropriate reference voltage ($V_{REFMD}$) can be determined for the MDAC circuit (via the evaluator circuit) prior to sampling the output of the SHA circuit ($V_{SHA}$). Since the SHA circuit is operated with a half clock latency, the MDAC reference voltage can be pre-sampled on the feedback capacitor ($C_{F2}$) during the sampling of the SHA circuit output. The input sampling signal can

20 amplified by a factor of two during the next sampling phase (signal $Q_1$) and the dropping voltage corresponds to the pre-sampled reference voltage.

    Since $V_{REFMD}$ is not fed into the sampling capacitor ($C_{S2}$), the dropping voltages of MDAC circuit at the tripping points are substantially independent of capacitor matching between the sampling capacitor ($C_{S2}$) and the feedback capacitor

25 ($C_{F2}$). The resulting voltage drops at the tripping points are approximately equal (e.g., 1V when +VREF and –VREF are =1V and -1V, respectively). Since no capacitor swapping is utilized, the signal transfer gains are approximately the same over the input range. Although variations in capacitor matching performance will result in transfer gain error, the transfer gain error does not deteriorate INL and DNL performance.

Mathematically, the transfer function resulting from the operation of the MDAC circuit described herein can be expressed as follows below.

For VIN < -¼ · VREF,

$$V_{OUT} = \left(1 + \frac{C_S}{C_F}\right) \cdot V_{IN} + 1 \qquad\qquad (Eq.11)$$

For -¼ · VREF < VIN < +¼ · VREF,

$$V_{OUT} = \left(\frac{C_S}{C_F}\right) \cdot V_{IN} \qquad\qquad (Eq.12)$$

For VIN > +¼ · VREF,

$$V_{OUT} = \left(\frac{C_S}{C_F}\right) \cdot V_{IN} - 1 \qquad\qquad (Eq.13)$$

Various performance merits of a pipelined converter circuit that is arranged in accordance with the present invention are illustrated in FIGS. 8 – 10.

FIG. 8 illustrates a residue voltage transfer curve for a non-ideal pipelined converter circuit that has a sampling capacitor ($C_S$) that is large relative to the feedback capacitor ($C_F$). The slope of the ideal transfer curve is noted by a dotted line in FIG. 8. The slope for the non-ideal pipelined converter does not change over the input range and the voltage drops at the tripping points in the transfer curve are approximately equal to one another. Since the slope is greater than two times, the input signal is amplified.

FIG. 9 illustrates a residue voltage transfer curve for a non-ideal pipelined converter circuit that has a sampling capacitor ($C_S$) that is small relative to the feedback capacitor ($C_F$). The slope of the ideal transfer curve is also noted by a dotted line in FIG. 9. The slope for the non-ideal pipelined converter does not change over the input range and the voltage drops at the tripping points in the transfer curve are approximately equal to one another. Since the slope is less than two times, the input signal is attenuated.

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FIG. 10 illustrates the conversion code transfer functions for ideal and non-ideal pipelined converters. The ideal transfer curve is illustrated as a dotted line. The non-ideal transfer curves for $C_S > 2 \cdot C_F$ and $C_S < 2 \cdot C_F$ illustrate a slope change in the transfer curves due to the non-ideal effects of mismatched capacitors.

5      The above specification, examples and data provide a complete description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.